A Circuit-Level Radiation Hardened-By-Design Approach for Standard CMOS

Completed Technology Project (2012 - 2015)

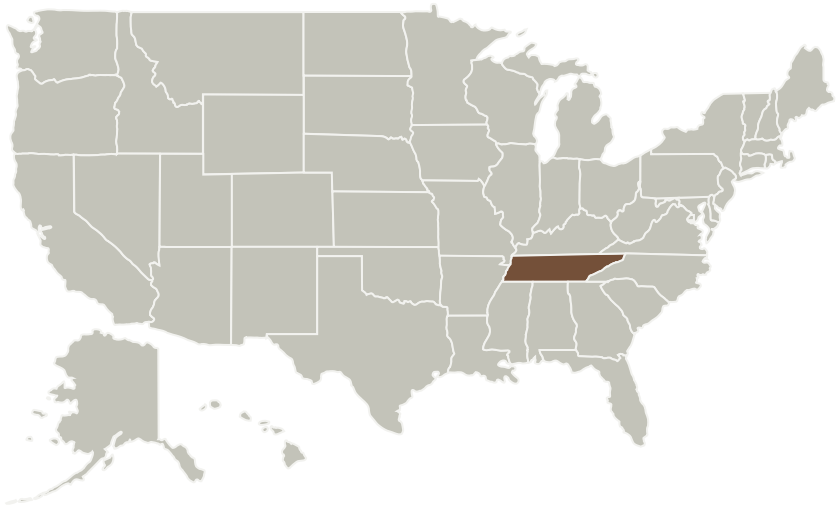
Project Introduction

The primary objective of the research inquiry is to validate a circuit-level radiation hardening technique for digital and mixed-signal electronics. Computer simulations have indicated that the technique works; however, there have been no published experimental results validating it. To complete the primary objective, there are plans to experimentally validate the hardening technique and to quantify its effectiveness and any performance degradation introduced by it. In comparison with many device-level hardening techniques, this circuit-level technique may reduce the development time and costs of digital or mixed-signal electronics in craft bound for radiation-rich environments such as space.

Anticipated Benefits

In comparison with many device-level hardening techniques, this circuit-level technique may reduce the development time and costs of digital or mixed-signal electronics in craft bound for radiation-rich environments such as space.

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
The University of Tennessee-Knoxville(UT-K)	Supporting Organization	Academia	Knoxville, Tennessee

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Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Responsible Program:

Space Technology Research Grants

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Primary U.S. Work Locations
Tennessee

Project Website:

https://www.nasa.gov/directorates/spacetech/home/index.html

Project Management

Program Director:
Claudia M Meyer

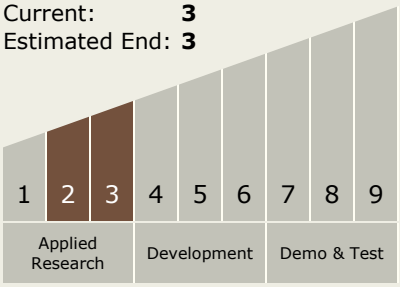
Program Manager:
Hung D Nguyen

Principal Investigator:
Ben Blalock

Co-Investigator:
Austin J Womac

Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **3**



Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.6 Radiation Hardened ASIC Technologies